CLAIM LISTING

This listing of claims will replace all prior versions, and listings of claims in the application:

AMENDMENTS TO THE CLAIMS

1.-3. (canceled)

4. (currently amended) The clamp circuit of Claim [[3]] 5, wherein the enable signal is asserted when the IC device operates in a first system that requires the I/O pin to be clamped during a voltage overshoot condition and the enable signal is de-asserted when the IC device operates in a second system that requires the I/O pin to be tri-stated.

5. (currently amended) ~~The clamp circuit of Claim 1,~~ A selectively enabled clamp circuit for limiting voltage overshoot on an input/output (I/O) pin of an associated integrated circuit (IC) device, comprising:

a single transistor connected between the I/O pin and ground potential and having a gate; and

means for controlling the conductive state of the single transistor in response to an enable signal;

wherein the means for controlling comprises:

a voltage detection circuit coupled to the I/O pin, the voltage detection circuit having an output terminal coupled to the gate of the single transistor and having an input terminal; and

a voltage level shifter circuit having a power terminal connected to the I/O pin, an output terminal coupled to the input terminal of the voltage detection circuit, and an input terminal to receive the enable signal.

6. (original) The clamp circuit of Claim 5, wherein the voltage detection circuit comprises:

first and second PMOS transistors connected in series between the I/O pin and the output terminal of the voltage detection circuit, the first PMOS transistor having a gate coupled to the output terminal of the level shifter circuit, and the second PMOS transistor having a gate coupled to a voltage supply of the IC device; and

a resistor connected between the output terminal of the voltage detection circuit and ground potential.

7. (original) The clamp circuit of Claim 6, wherein the voltage detection circuit turns on the single transistor when voltage on the I/O pin is greater than a sum of a threshold voltage of the second PMOS transistor and the voltage supply of the IC device if the enable signal is asserted.

8. (original) The clamp circuit of Claim 7, wherein the level shifter circuit turns on the first PMOS transistor when the enable signal is asserted and turns off the first PMOS transistor when the enable signal is de-asserted.

9. (currently amended) ~~The clamp circuit of Claim 1,~~ A selectively enabled clamp circuit for limiting voltage overshoot on an input/output (I/O) pin of an associated integrated circuit (IC) device, comprising:

a single transistor connected between the I/O pin and ground potential and having a gate; and

means for controlling the conductive state of the single transistor in response to an enable signal;

wherein the means for controlling comprises:

a PMOS transistor connected between the I/O pin and an intermediate node and having a gate coupled to a voltage supply of the IC device; and

a voltage level shifter circuit having a power terminal connected to the intermediate node, an output terminal coupled to the gate of the single transistor, and an input terminal to receive the enable signal.

10. (original) The clamp circuit of Claim 9, further comprising:

a resistor connected between the gate of the single transistor and ground potential.

11. (original) The clamp circuit of Claim 9, wherein the level shifter circuit turns on the single transistor when voltage on the I/O pin is greater than a sum of a threshold voltage of the PMOS transistor and the voltage supply of the IC device if the enable signal is asserted.

12. (original) The clamp circuit of Claim 11, wherein the level shifter circuit maintains the single transistor in a non-conductive state if the enable signal is de-asserted.

13. (original) A selectively enabled clamp circuit for limiting voltage overshoot on an input/output (I/O) pin of an associated integrated circuit (IC) device, comprising:

a discharge circuit connected between the I/O pin and ground potential;

a voltage detection circuit coupled to the I/O pin, the voltage detection circuit having an output terminal coupled to the discharge circuit and having an input terminal; and

a voltage level shifter circuit having a power terminal connected to the I/O pin, an output terminal coupled to the input terminal of the voltage detection circuit, and an input terminal to receive an enable signal.

14. (original) The claim circuit of Claim 13, wherein the discharge circuit comprises a single NMOS transistor connected between the I/O pin and ground potential and having a gate; and

wherein the output terminal of the voltage detection circuit is coupled to the gate of the single transistor.

15. (original) The clamp circuit of Claim 14, wherein the voltage detection circuit comprises:

first and second PMOS transistors connected in series between the I/O pin and the output terminal of the voltage detection circuit, the first PMOS transistor having a gate coupled to the output terminal of the level shifter circuit, and the second PMOS transistor having a gate coupled to a voltage supply of the IC device; and

a resistor connected between the output terminal of the voltage detection circuit and ground potential.

16. (original) The clamp circuit of Claim 15, wherein the voltage level shifter circuit turns on the NMOS transistor when voltage on the I/O pin is greater than a sum of a threshold voltage of the second PMOS transistor and the voltage supply of the IC device if the enable signal is asserted.

17. (original) The clamp circuit of Claim 15, wherein the voltage level shifter circuit maintains the NMOS transistor in a non-conductive state when the enable signal is de-asserted.

18. (original) The clamp circuit of Claim 15, wherein the level shifter circuit turns on the first PMOS transistor when the enable signal is asserted and turns off the first PMOS transistor when the enable signal is de-asserted.

19. (original) A selectively enabled clamp circuit for limiting voltage overshoot on an input/output (I/O) pin of an associated integrated circuit (IC) device, comprising:

a discharge circuit connected between the I/O pin and ground potential;

a PMOS transistor connected between the I/O pin and an intermediate node and having a gate coupled to a voltage supply of the IC device; and

a voltage level shifter circuit having a power terminal connected to the intermediate node, an output terminal coupled to the discharge circuit, and an input terminal to receive an enable signal.

20. (original) The claim circuit of Claim 19, wherein the discharge circuit comprises a single NMOS transistor connected between the I/O pin and ground potential and having a gate; and

wherein the output terminal of the voltage level shifter circuit is coupled to the gate of the single transistor.

21. (original) The clamp circuit of Claim 20, further comprising:

a resistor connected between the gate of the NMOS transistor and ground potential.

22. (original) The clamp circuit of Claim 20, wherein the level shifter circuit turns on the NMOS transistor when voltage on the I/O pin is greater than a sum of a threshold voltage of the PMOS transistor and the voltage supply of the IC device if the enable signal is asserted.

23. (original) The clamp circuit of Claim 20, wherein the level shifter circuit maintains the NMOS transistor in a non-conductive state if the enable signal is de-asserted.

24.-28. (canceled)

29. (new) The clamp circuit of Claim 9, wherein the enable signal is asserted when the IC device operates in a first system that requires the I/O pin to be clamped during a voltage overshoot condition and the enable signal is de-asserted when the IC device operates in a second system that requires the I/O pin to be tri-stated.